REMARKS

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

Claims 1-13 were presented for consideration in this application. By the foregoing amendment, Applicant has amended Claims 8 and 11. Claims 1-13 are still pending.

Applicant thanks the Examiner for acknowledgment of applicant's claim for foreign priority based on an application filed in EPO on 8/21/00 and 5/11/01. Applicant mailed certified copies on March 7, 2003.

The specification is amended to update the status of the related US patent applications referred to on page 1, as requested.

Claim 8 is amended to correct a grammar error. Claim 11 is amended for clarity.

Rejections

Claims 1-2, 8, and 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. (Chang) US Patent No. 6,289,414.

The Examiner characterizes Chang as teaching:

> *incorporating a task ID value (Fig. 5 and col. 10 line 35); and locking or unlocking a portion if the plurality of translated memory address in the TLB such that only an entry of a selected program task in the plurality of translated memory addresses is affected (Fig. 5 lock bits and col. 9 lines 48-54).*

Applicant respectfully disagrees with the characterization of Chang. Applicant agrees that Chang does have a field in the translation lookaside buffer (TLB) that holds "lockbits;" however, Chang's lockbits perform a completely different function than claimed in Applicant's method base claim 1 and system base claim 8. Chang's lockbits are used to protect persistent storage:

> Support for a Persistent Storage class is provided by a set of "lock bits" associated with each virtual page. The lock bits effectively extend the storage protection granularity to "lines" of storage (128-bytes for 2K pages, or 256-bytes for 4K pages) and allow the operating system to detect and automatically journal changes to Persistent variables. Persistent Storage class as used herein means storage which may reside permanently on disk file storage. (Col 9, lines 21-29)

> Lockbit: One of a set of 16 bits associated with each page of a Persistent Storage segment. Each lockbit is associated with one Line of storage. The combination of Transaction ID, the Write bit, and the Lockbit value for a Line determine whether a storage access request is granted or denied in a Persistent Storage segment. (col 9, lines 49-54)

Locking a line of memory of page in memory that holds program data is completely different from "locking or unlocking a portion of the plurality of **translated memory address in the TLB** in a manner that is qualified by the task identification value" as recited in Claim 1. Similarly, base Claim 8 recites: "...the **TLB** comprising: storage circuitry with a **plurality of entry locations** ... wherein the control circuitry is responsive to an operation command to lock or unlocked selected ones of the plurality of **entry locations** which have a first qualifier value in the second field." Base Claims 1 and 8 are allowable over Chang for this reason.

Chang's TLB does have a transaction ID (TID) (Col 10, lines 35-38), but Applicant finds no suggestion to lock or unlock TLB entries "in a manner that is **qualified by** the task identification value" as recited by Claim 1 or "responsive to an **operation command** to lock or unlock selected ones of the plurality of entry locations which have a first qualifier value" as recited in base Claim 8. The fact the Chang has a field for TID does not suggest that this field qualifies the operation of any command that affects TLB entries. Base Claims 1 and 8 are therefore allowable over Chang for this additional reason.

Claim 10 has been amended to clarify the "resource ID" refers to "requester resource ID" to identify a resource that requests a memory transaction, as discussed in paragraph [25] of the application. Chang has no suggestion of "control circuitry is responsive to an operation command to lock or unlock selected ones of the plurality of entry locations which have both a specified task ID value in the second field and a specified **requester resource ID** value in the third field. The Examiner pointed to a segment ID, but this is just part of the address. (Col 10, lines 35-38)

Regarding Claim 11, since Chang's lockbits do not control TLB entries, Chang does not suggest "skip circuitry operable to cause the shift register to skip over locked entry locations."

Regarding Claim 12, since Chang's lockbits do not control TLB entries, Chang does not suggest "reservation circuitry operable to reserve a portion of the entry locations from being locked."

Claims 1-7 and 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond et al. (Hammond) US Patent No. 5,940,872 in view of Mohamed et al. (Mohamed) US Patent No. 5,899,994 or Ganapathy et al. (Ganapathy) US Patent No. 6,182,089.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond et al. (Hammond) US Patent No. 5,940,872 in view of Mohamed et al. (Mohamed) US Patent No. 5,899,994 or Ganapathy et al. (Ganapathy) US Patent No. 6,182,089 and further in view of Woolsey et al. (Woolsey) US Patent No. 6,029,000.

Regarding Hammond, Applicant agrees with the Examiner that Hammond does not specifically disclose the step of incorporating a task ID value. Mohamed uses a "process ID" but only in the first TLB entry "to indicate the physical location of the user TSB for the currently running user process" and in the last TLB entry: "A last entry 320 of TLB 302 is dedicated to mapping the kernel. Process identifier 322 identifies the kernel process ...." (Col 8, lines 32-34 and 51-53) Thus, Mohamed does not have any suggestion regarding "locking or unlocking a portion of the plurality of translated memory address in the TLB in a manner that is qualified by the task identification value, such that only an entry of a selected program task in the plurality of translated memory addresses is affected" as recited in Claim 1 or similarly in base Claim 8.

Ganapathy does have a process ID (PID) in each TLB entry. (Col. 8, lines 40-49) Ganapathy notes: "Because TLB flushes are costly, it is advantageous to limit them as much as possible." (Col. 18, lines 3-4) Having noted this, Ganapathy has no teaching regarding use of the PID to "such that only an entry of a selected program task in the plurality of translated memory addresses is affected" as recited by Claim 1 and similarly by base Claim 8. Ganapathy teaches:

> It should be noted that if mapped data is moved (or "migrated") from a first page in memory to a second page in memory, any copies of page table entries that reference the memory page, including copies placed in a TLB, must be flushed or invalidated. PTEs that reference the first page are generally updated to reference the second page. If mapped data is deleted, page table entries that reference the page are typically invalidated. (Col. 9, lines 1-8)

Again, Ganapathy makes no suggestion of using the PID field to manage this operation of invalidating entries, so there is no motivation for combing Ganapathy with Hammond to arrive at a system that performs "locking or unlocking a portion of the plurality of translated memory address in the TLB in a manner that is qualified by the task identification value" as recited by Claim 1 and similarly in base Claim 8. Thus, base Claims 1 and 8 are allowable over Hammond, Mohamed and Ganapathy in any combination.

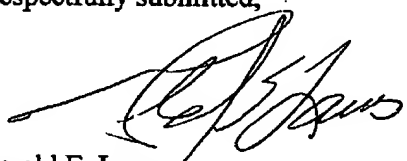
Dependent Claims 2-7 and 9-13 depend directly or ultimately on an allowable base Claim and are therefore allowable for this reason and by virtue of their further distinctive recitations. For example, Claim 2 recites: "locking or unlocking **only and all** of the plurality of translated addresses that have the selected task identification value." As discussed above, neither Mohamed nor Ganapathy suggest using the process identifier to manage the TLB, therefore there is no suggestion to lock or unlock all TLB entries of a particular task based on the task ID in the TLB entries.

Regarding Claims 7 and 12, Examiner points to Hammond, Col 7, lines 25-28; however, Applicant finds nothing in Hammond that suggests "reserving a portion of the entry locations from being locked" as described in the application at paragraph [91] and elsewhere.

Applicant believes this application and the claims herein to be in a condition for allowance and respectfully requests that the Examiner allow this application to pass to the issue branch.

Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,



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